SONY® **CXP50112/50116**

CMOS 4-bit 1 Chip Microcomputer

Description

CXP50112/CXP50116 is a CMOS 4-bit microcomputer which consists of 4-bit CPU, ROM, RAM, I/O port, 8-bit timer, 8-bit timer/counter, 18-bit time base timer, 8-bit serial I/O, vector interruption, power on reset function, fluorescent display tube controller/driver, D/A conversion PWM output port, a remote control reception circuit, 3-bit A/D converters, a 32kHz timer/event counter and a power supply current detection reset function. They are integrated into a single chip with the standby function, etc. which are to be operated at a low power consumption.

80 pin QFP (Plastic)

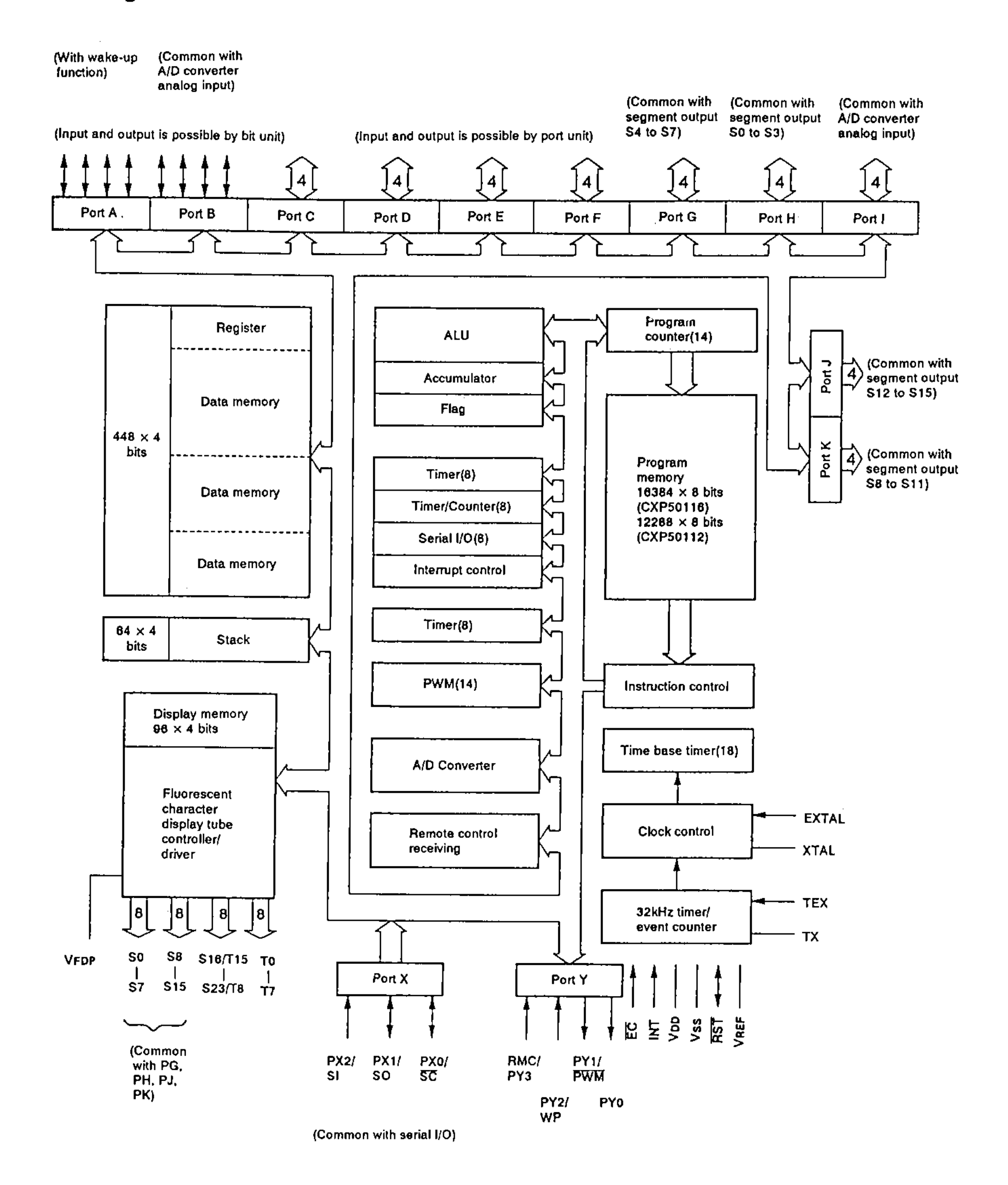
Structure

Silicon gate CMOS IC

Features

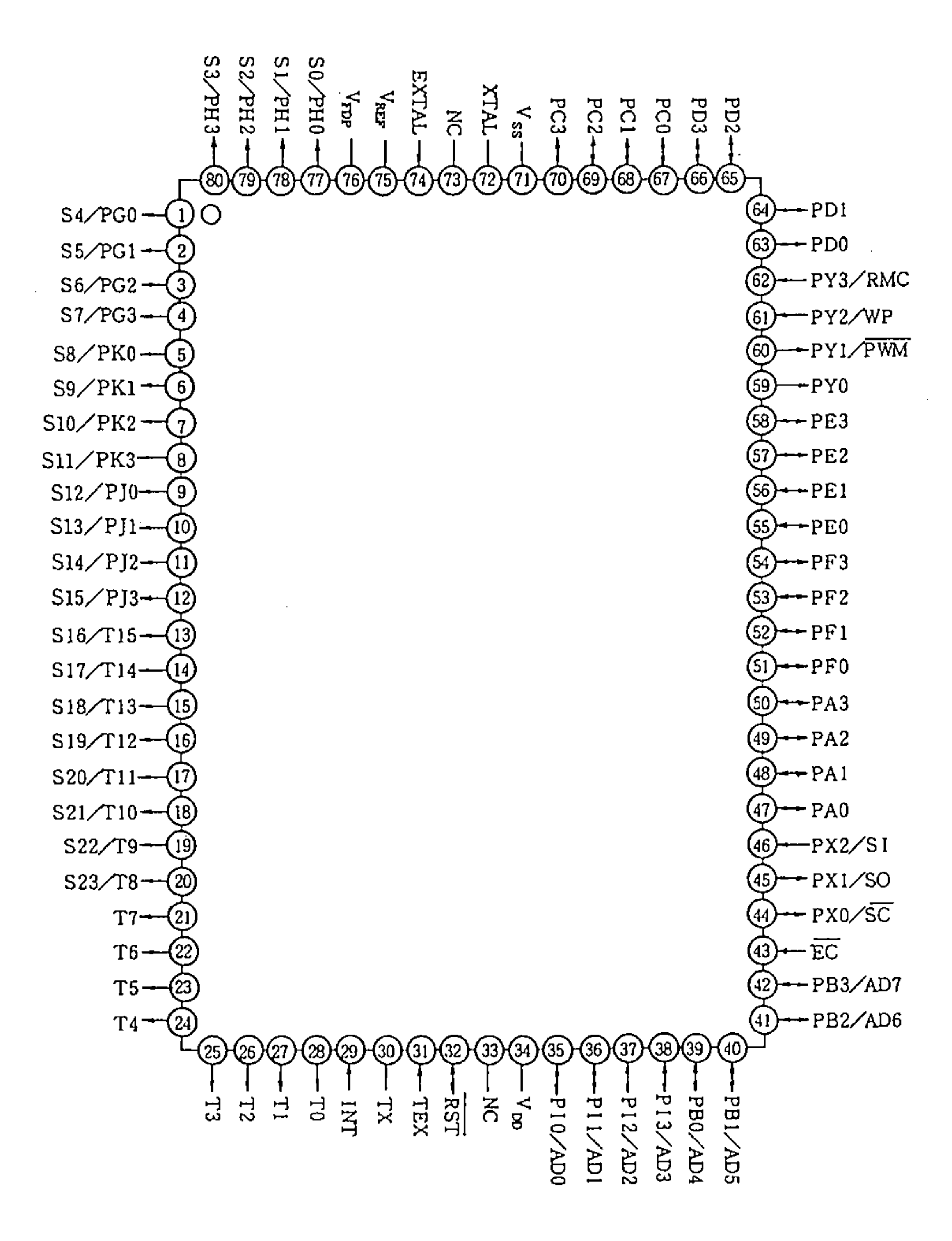
- Instruction cycle 1.9 μs/4.19MHz
  122 μs/32kHz
  (Selection possible for program)
- ROM capacity 16,384 × 8 bits (CXP50116)
  12,288 × 8 bits (CXP50112)
- RAM capacity 554 × 4 bits (Including display area)
- 51 general purpose I/O ports
- Fluorescent display tube controller/driver (Ables to display maximum 256 segments)
  - 1 to 16 digits dynamic scan display (1 to 8 digits at 24 segments)
  - Page mode/variable mode
  - Dimmer function
  - High tension proof output (40V)
  - Selection possible for incorporating pull-down resistance (mask option)
- 14-bit PWM output for D/A conversion
- Remote control receiving circuit (Independ the timer/counter)
- 3-bit A/D converter (8 channels per circuit)
- 32kHz reload timer/event counter
- Power supply voltage detection reset function (mask option)
- Rich wake-up functions WP pin 4 general purpose ports (edge detection)
  32kHz timer/counter Remote control receiving circuit
- 8-bit/4-bit variable prescaler serial I/O
- 8-bit prescaler timer, 8-bit prescaler timer/event counter and 18-bit time base timer, 8-bit reload type timer with prescaler, independently controlled
- Arithmetic and logical operations possible between the entire RAM area, I/O area and the accumulator by means of memory mapped I/O
- Reference to the entire ROM area is possible with the table look-up instruction
- 2 kinds of power down modes of sleep and stop
- Power on reset circuit (mask option)
- Provided with 80 pin plastic QFP
- Provided with 80 pin piggyback QFP (CXP50100)

Block Diagram



Pin Configuration Diagram (Top View)

Note) Do not make any connections to NC pins.



Pin Description

Symbol	Name	I/O	Equivalent Circuit	Description
VDD	Supply voltage	—		Positive voltage supply pin
Vss	Grounding voltage	—		GND pin
EXTAL	Clock input	I		Clock oscillation circuit input pin. Connect the crystal oscillator or ceramic resonator between the EXTAL and XTAL. To use an external clock input, connect the clock oscillation source to the EXTAL pin and open the XTAL pin.
XTAL	Clock output	O		Clock oscillation circuit output pin
$\overline{RST}$	Reset	I/O	Mask option Output pull-up resistor (P-ch Tr) N-ch Tr output Schmitt inverter input	Serves as the incorporated power-on reset circuit output pin. When inputting a reset signal from the outside, provide 2 instruction cycles or longer of an "L" level (0V).
INT	External interrupt	I		Serves as interrupt input pin. Permits the selection with a program of the edge and the level modes.
$\overline{EC}$	Event counter input	I		Event counter input pin.
SI/PX2	Serial input Port X	I	Schmitt inverter input	Doubles as a serial interface (8 bits) input pin and as bit "2" (input) of port X.
SO/PX1	Serial output Port X	I/O	Tri-state output or pull-up resistor output possible Inverter input	Doubles as a serial interface (8 bits) output pin and as bit "1" (input) of port X.
$\overline{SC}$/PX0	Serial clock Port X	I/O	Tri-state output or pull-up resistor output possible Inverter input	Doubles as clock input/output pin for the serial interface and as bit "0" (input) of port X.

Symbol	Name	I/O	Equivalent Circuit	Description
RMC/PY3	Remote control input Port Y	I	Schmitt inverter input	Remote control receiver input pin. Input pin for bit "3" of port Y.
WP/PY2	Wake-up input Port Y	I		Doubles as a wake-up input pin to release the standby state, and as bit "2" (input) of port Y..
$\overline{PWM}$/PY1	PWM output Port Y	O	(When reset: 1) Inverter output	Doubles as a PWM generator (14 bits) output and as bit"1" (output) of port Y.
PY0	Port Y	O		Output pin for bit "0" of port Y.
PA0 to PA3	Port A	I/O	B and I only for A/D input port Tri-state output or pull-up resistor output possible Inverter input	This 4-bit input/output port permits its each individual port to be programmed to serve for input or output. Its output format is a tristate or pull-up resistor output.
PB0/AD4 to PB3/AD7	Analog input Port B	I/O		This 4-bit input/output port permits its each individual bit to be programmed to serve either as input or output. Its output format is a tri-state or pull-up resistor output. It is also used for A/D converter input.
PC0 to PC3	Port C	I/O		This 4-bit input/output port permits its each individual port to be programmed to serve for input or output. Its output format is a tristate or pull-up resistor output.
PD0 to PD3	Port D	I/O		This 4-bit input/output port has the functions that are equivalent to those of port C.
PE0 to PE3	Port E	I/O		This 4-bit input/output port has the functions that are equivalent to those of port C.
PF0 to PF3	Port F	I/O		This 4-bit input/output port has the functions that are equivalent to those of port C.
PI0/AD0 to PI3/AD3	Analog input Port I	I/O		This 4-bit input/output port has the functions that are equivalent to those of port C. It is also used for A/D converter input.

Symbol	Name	I/O	Equivalent Circuit	Description
V_{FDP}	Power supply for FDP	—		Load current supply pin needed when load resistance is built-in to output driver for FDP (Fluoresent display pannel).
T0 to T7	Timing	O	P-ch open drain output Pull-down resistance (Mask option)	Lower 8-digit output pin of the FDP timing signal.
T8/S23 to T15/S16	Timing/segment	O		Combination output pin of higher 8-digit of the FDP timing signal and the segment signal.
PG0/S4 to PG3/S7	Port G/segment	O		Combination pin of the 4-bit output port and FDP segment signal output.
PH0/S0 to PH3/S3	Port H/segment	O		The same as port G.
PJ0/S12 to PJ3/S15	Port J/segment	O		The same as port G.
PK0/S8 to PK3/S11	Port K/segment	O		The same as port G.
TEX	32kHz T/C clock input	I	Mask option	Input pin of the 32kHz timer clock generated circuit. Connect 32,768kHz crystal oscillator between TEX and TX. Connect clock oscillation source to TEX pin and bleed TX pin when this circuit is used as event clock input.
TX	32kHz T/C clock output	O		Output pin of the clock generated circuit.
V_{REF}	Reference voltage input	I		Reference voltage input for power supply voltage resetting circuit. Connect the zener diode normally.

Absolute Maximum Ratings

(Ta=–20 to +75°C, Vss=0V)

Item	Symbol	Rating	Unit	Remarks
Power supply voltage	V_{DD}	–0.3 to +7.0	V	
Input voltage	V_{IN}	–0.3 to +7.0 *1	V	
Output voltage	V_{OUT}	–0.3 to +7.0 *1	V	
Display output voltage	V_{OD}	V_{DD}–40 to V_{DD}+0.3	V	As P channel transistor is open drain, V_{DD} voltage is determined as standard.
High level output current	I_{OH}	–5	mA	Other than display output pins *2 : per pin
	I_{ODH1}	–15	mA	Display output S0 to S15 : per pin
	I_{ODH2}	–35	mA	Display output T0 to T7, T8/S23 to T15/S16 : per pin
High level total output current	ΣI_{OH}	–40	mA	Total of other than display output pins
	ΣI_{ODH}	–100	mA	Total of display output pins
Low level output current	I_{OL}	15	mA	Port 1 pin
	I_{OLC}	20	mA	High current port pin *3
Low level total output current	ΣI_{OL}	100	mA	Entire pin total
Operating temperature	Topr	–20 to +75	°C	
Storage temperature	Tstg	–55 to +150	°C	
Allowable power dissipation	P_D	600	mW	QFP

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should better take place under the recommended operation conditions. Exceeding those conditions may adversely affect the reliability of the LSI.

*1) V_{IN} and V_{OUT} should not exceed V_{DD}+0.3V.

*2) Specifies the output current of the general purpose I/O port PA to PF, PI, SO, $\overline{SC}$, PY0 and PY1.

*3) The high current operation transistors are the N-CH transistors of the PC and PD ports.

Recommended Operating Condition

(Vss=0V)

Item	Symbol	Min.	Max.	Unit	Remarks
Power supply voltage	V_{DD}	4.5	5.5	V	Guaranteed range of operation by EXTAL colck
		2.5	5.5	V	Guaranteed range of operation by TEX colck, guaranteed range of data hold during STOP
High level input voltage	V_{IH}	0.7V_{DD}	V_{DD}	V	
	V_{IHS}	0.8V_{DD}	V_{DD}	V	Hysteresis input *1
	V_{IHEX}	V_{DD}–0.4	V_{DD}+0.3	V	EXTAL pin *2
Low level input voltage	V_{IL}	0	0.3V_{DD}	V	
	V_{ILS}	0	0.2V_{DD}	V	Hysteresis input *1
	V_{ILEX}	–0.3	0.4	V	EXTAL pin *2
Operating temperature	Topr	–20	+75	°C	

*1) The TEX pin when the counter mode is selected by each of INT, $\overline{EC}$, PX0, PX2, PY2, PY3, $\overline{RST}$ pins and mask option.

*2) Specified only during external clock input.

Electrical Characteristics

DC characteristics

(Ta=–20 to +75°C, Vss=0V)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
High level output voltage	V_{OH}	PA to PF, PI PX0, PX1 PY0, PY1 $\overline{RST}$ (V_{OL} only)	V_{DD}=4.5V, I_{OH}=–0.5mA	4.0			V
			V_{DD}=4.5V, I_{OH}=–1.0mA	3.5			V
Low level output voltage	V_{OL}		V_{DD}=4.5V, I_{OL}=1.8mA			0.4	V
			V_{DD}=4.5V, I_{OL}=3.6mA			0.6	V
		PC, PD	V_{DD}=4.5V, I_{OL}=12mA			1.5	V
Input current	I_{IHE}	EXTAL	V_{DD}=5.5V, V_{IH}=5.5V	0.5		40	µA
	I_{ILE}		V_{DD}=5.5V, V_{IL}=0.4V	–0.5		–40	µA
	I_{IHT}	TEX*3	V_{DD}=5.5V, V_{IH}=5.5V	0.1		10	µA
	I_{ILT}		V_{DD}=5.5V, V_{IL}=0.4V	–0.1		–10	µA
	I_{ILR}	$\overline{RST}$*2		–1.5		–400	µA
High impedance I/O leakage current	I_{IZ}	PA to PF, PI PX0 to PX2, PY2, PY3, $\overline{EC}$, INT, $\overline{RST}$*2, TEX*3	V_{DD}=5.5V V_I=0, 5.5V			±10	µA
Display output current	I_{OH}	S0 to S15	V_{DD}=4.5V V_{OH}=V_{DD}–2.5V	–7			mA
		S16/T15 to S23/T8, T0 to T7		–18			mA
Open drain output leakage current (P-CH Tr OFF in state)	I_{LOL}	S0 to S15, S16/T15 to S23/T8, T0 to T7	V_{DD}=5.5V V_{OL}=V_{DD}–35V			–20	µA
Pull-down resistance*1	R_L	S0 to S15, S16/T15 to S23/T8, T0 to T7	V_{DD}=5V V_{FDP}=V_{DD}–35V	60	100	270	kΩ
Supply current	I_{DD1}	V_{DD}	Entire output pins open Crystal oscillation (C1=C2=22pF) of V_{DD}=5.5V, 4.19MHz		7	20	mA
	I_{DD2}		Crystal oscillation (C1=C2=18pF) of V_{DD}=3V, 32kHz		50	250	µA
	I_{DDSP1}		SLEEP mode V_{DD}=5.5V, 4.19MHz oscillation		5	12	mA
	I_{DDSP2}		V_{DD}=3V, 32kHz oscillation		40	200	µA
	I_{DDS1}		STOP mode V_{DD}=3V, 32kHz with T/C		7	40	µA
	I_{DDS2}		V_{DD}=5.5V, 32kHz without T/C (For mask option select counter, Pin is fixed.)			10	µA
Input capacity	C_{IN}	PA to PF, PI, PX, PY2, PY3, EXTAL, TEX, $\overline{EC}$, INT, $\overline{RST}$	Clock 1MHz 0V other than the measured pins		10	20	pF

* 1) In case the incorporated pull-down resistance has been selected with mask option.
* 2) $\overline{RST}$ pin specifies the input current when the pull-up resistance is selected, and specifies leakage current when nonresistance is selected.
* 3) The TEX pin specifies the input current when the 32kHz oscillation is selected by the mask option, and specifies the leak current when the counter mode is specified.

AC Characteristics

(1) Clock timing (Ta=–20 to +75 °C, V_{DD}=4.5V to 5.5V, Vss=0V)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
System clock frequency	fc	XTAL EXTAL	Fig. 1, Fig. 2	1		5	MHz
System clock input pulse width	t_{XL} t_{XH}	EXTAL	Fig. 1, Fig. 2 (External clock drive)	90			ns
System clock input rising and falling times	t_{CR} t_{CF}	EXTAL	Fig. 1, Fig. 2 (External clock drive)			200	ns
System clock frequency	fcs	TEX *2 TX	V_{DD}=2.5 to 5.5V Fig. 2		32.768		kHz
Event count clock input pulse width	t_{EL} t_{EH}	$\overline{EC}$	Fig. 3	tsys *1 +0.05			µs
Event count clock input rising and falling times	t_{ER} t_{EF}	$\overline{EC}$	Fig. 3			20	ms
Event count input clock input pulse width	t_{TL} t_{TH}	TEX *3	Fig. 3	10			µs
Event count input clock rising and falling times	t_{TR} t_{TF}	TEX *3	Fig. 3			20	ms

* 1) tsys in the EXTAL input clock is tsys=8/fc
tsys in the TEX input clock is tsys=4/fcs
* 2) Specified when the crystal oscillation mode is selected by the mask option.
* 3) Specified when the counter mode is selected by the mask option.

Note) When adjusting the frequency accurately, there may be cases in which they may differ from Fig. 2.

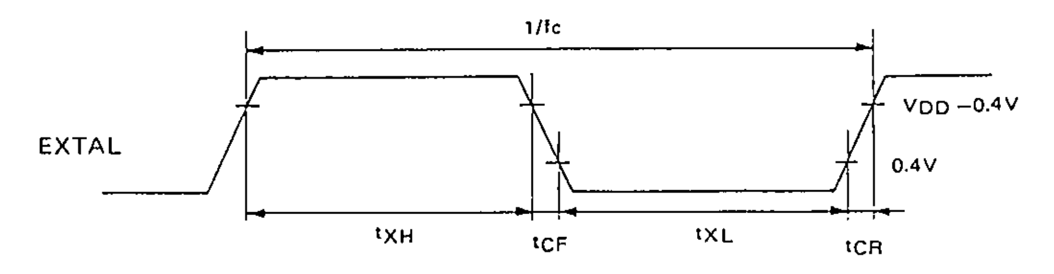


Fig. 1. Clock timing

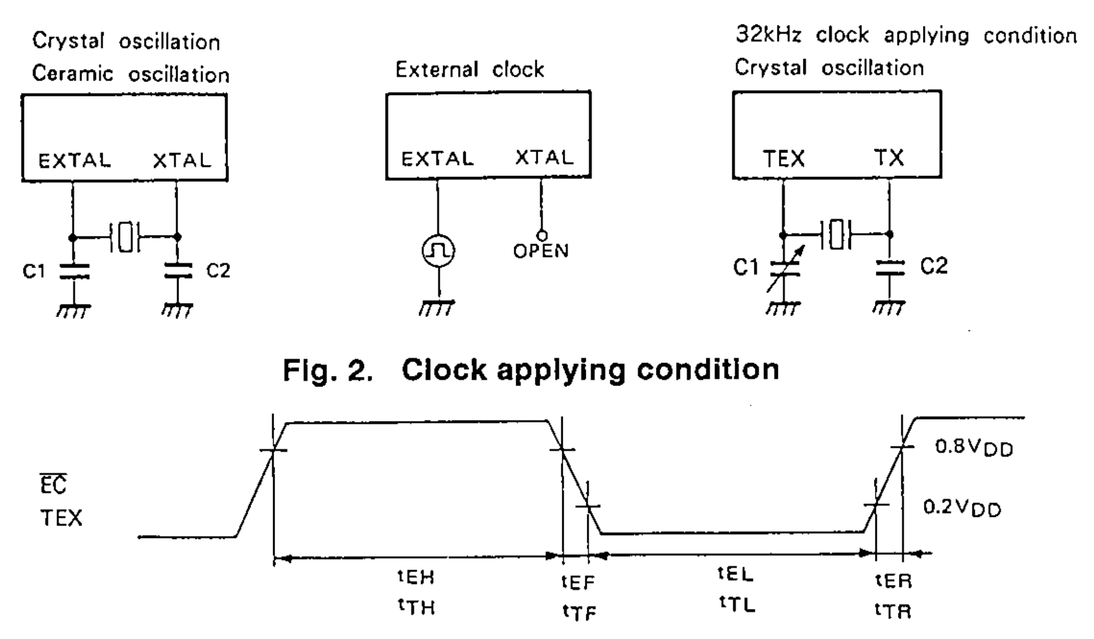


Fig. 2. Clock applying condition

Fig. 3. Event count clock timing

(2) Serial transfer (Ta=–20 to +75°C, VDD=4.5V to 5.5V, Vss=0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
Serial transfer clock ($\overline{SC}$) cycle time	tKCY	$\overline{SC}$	Input mode	tsys/4 + 1.42		µs
			Output mode	tsio		µs
Serial transfer clock ($\overline{SC}$) high and low level widths	tKH tKL	$\overline{SC}$	Input mode	tsys/8 + 0.7		µs
			Output mode	tsio/2 – 0.1		µs
Serial data input setup time (against $\overline{SC}$ ↑)	tSIK	SI	$\overline{SC}$ input mode	0.1		µs
			$\overline{SC}$ output mode	0.2		µs
Serial data input hold time (against $\overline{SC}$ ↑)	tKSI	SI	$\overline{SC}$ input mode	tsys/8+0.5		µs
			$\overline{SC}$ output mode	0.1		µs
Data delay time from $\overline{SC}$ falling	tKSO	SO			tsys/8 + 0.5	µs

Note 1) tsys is the EXTAL input clock tsys=8/fc
(It cannot be used with TEX input clock)
tsio in turned into either 2tsys, 4tsys or 16tsys by means of a program
2) The Load of data output delay is 50pF + 1TTL

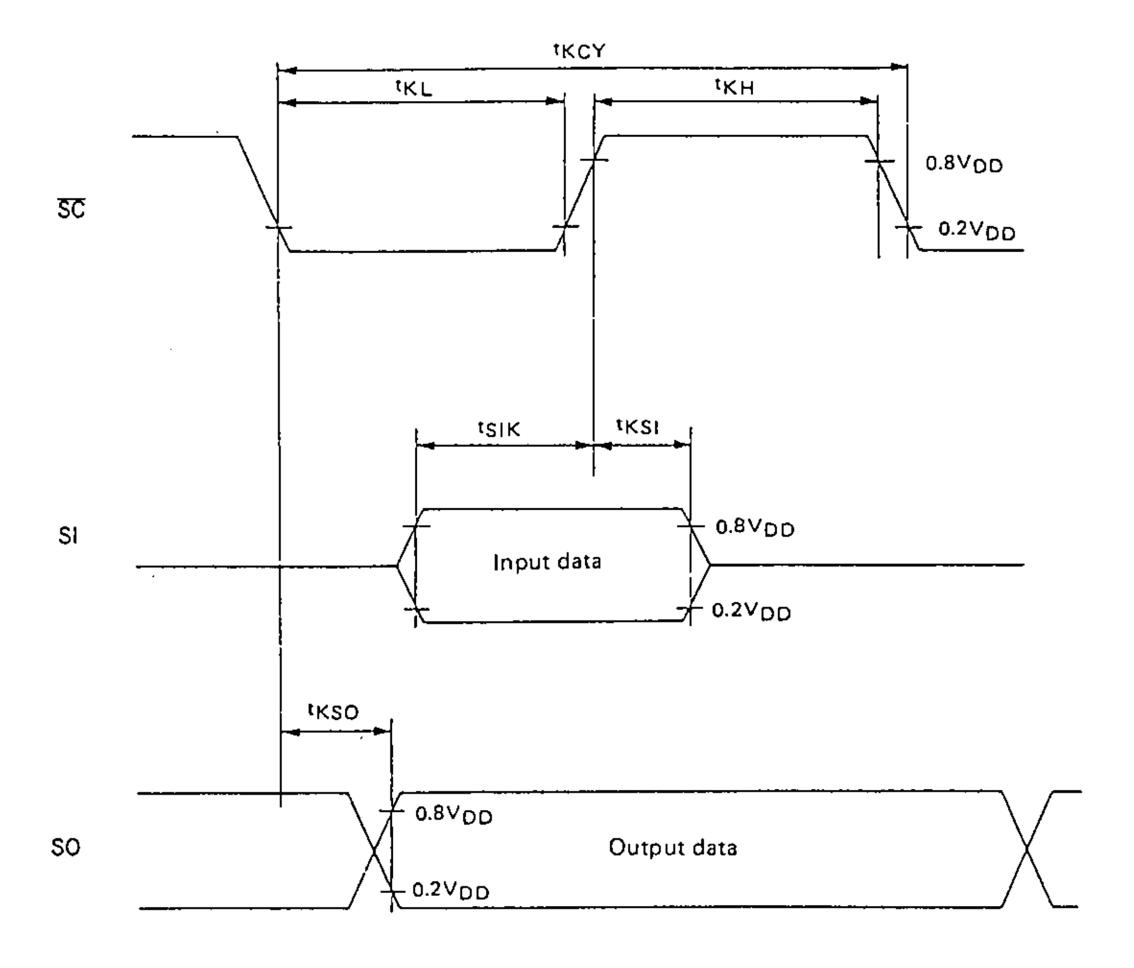


Fig. 4. Serial transfer timing

(3) A/D converter (Ta=–20 to +75°C, Vss=0V)

Analog input voltage	Pin	Condition	Digital conversion value
0.0 to 0.33V	AD0 to AD7	V_{DD}=5V	000
0.82 to 1.29V			001
1.78 to 2.21V			010
2.69 to 3.06V			011
3.56 to 4.06V			100
4.62 to 5.0V			101

Note) The digital conversion value are the values when FF_H address of the RAM file 1 in the program are read.

(4) Power Supply Voltage Detection Reset Function (Ta=–20 to +75°C, Vss=0V)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Power supply voltage detection reset function of operation voltage range	V_{LPOP}	V_{DD}	Voltage range allowing system operation	2.5		5.5	V
Power supply voltage drop detection function	V_{POP}	V_{DD}	When V_{REF} pin voltage is 3.3V Flag set when voltage drops System reset when voltage rises	3.8	4.0	4.2	V

The graph in Fig. 5 shows the relationship between the power supply voltage V_{DD} and reference voltage V_{REF} of the power supply voltage detection reset function.

Note) The graph in Fig. 5 serves as guide to the function operation area obtained using average devices.
Individual adjustment is needed when Zener diodes, etc., are connected to the V_{REF} pin.

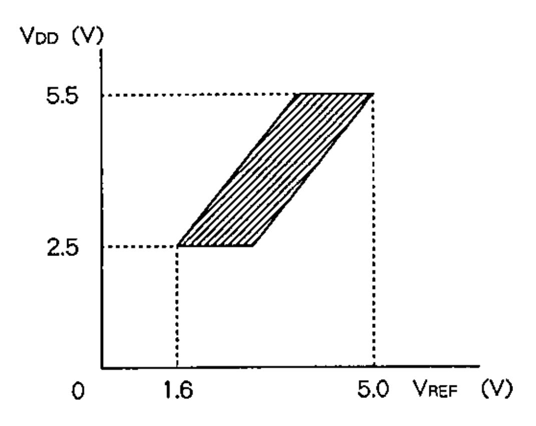


Fig. 5 Power supply voltage detection reset function chart

(5) Others (Ta=–20 to +75°C, V_{DD}=4.5V to 5.5V, Vss=0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
External interruption high and low level widths	t_{I1H}, t_{I1L}	INT	During edge detection mode	tsys + 0.05		µs
Reset input low level width	t_{RSL}	$\overline{RST}$		2tsys *1		µs
Wake-up input high level width	t_{WPH}	WP	STOP mode	500		ns
			SLEEP mode	tsys + 0.05		µs
Wake-up input high and low level widths	t_{WPAH} t_{WPAL}	PA0 to PA3	STOP mode	500		ns
			SLEEP mode	500		ns

Note) tsys in the EXTAL input clock is 8/fc

*1) For resetting when operating in TEX input clock, hold the low level more than the oscillation stabilizing time of EXTAL input clock.

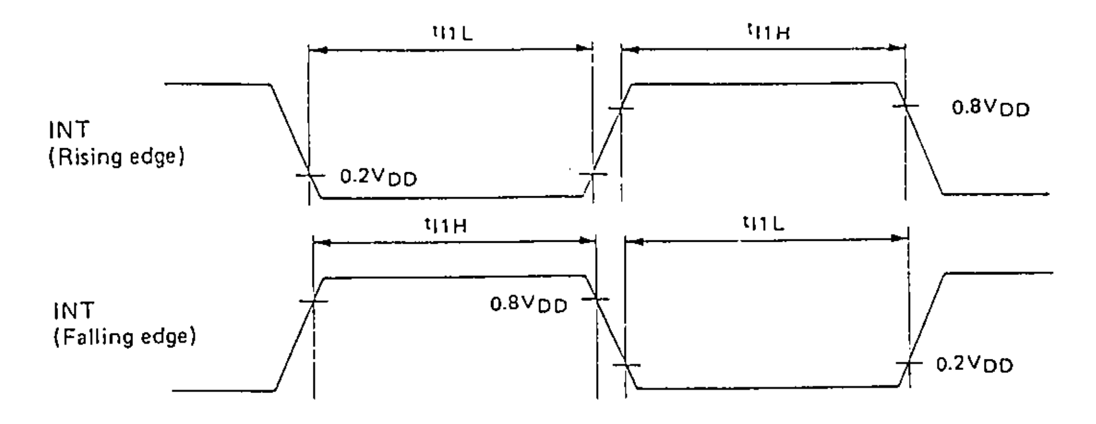


Fig. 6. Interruption input timing

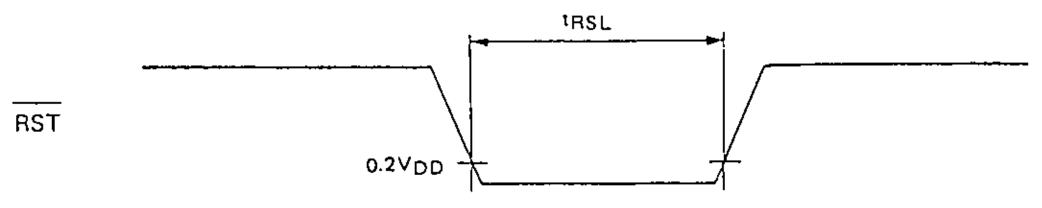


Fig. 7. Reset input timing

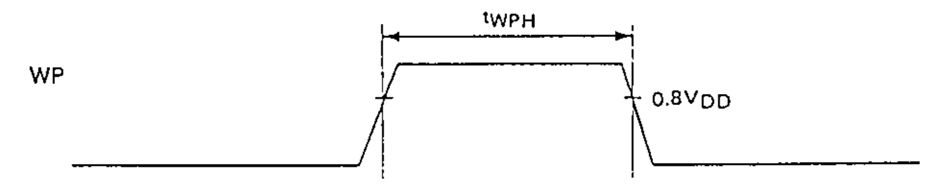


Fig. 8. Wake-up input timing

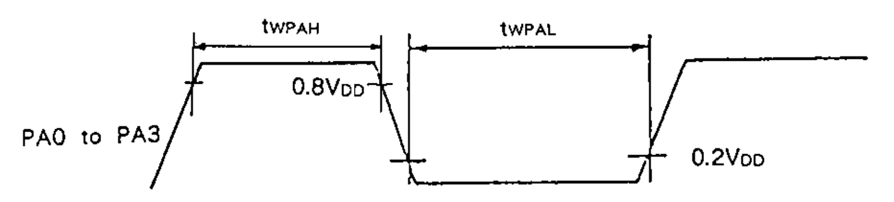


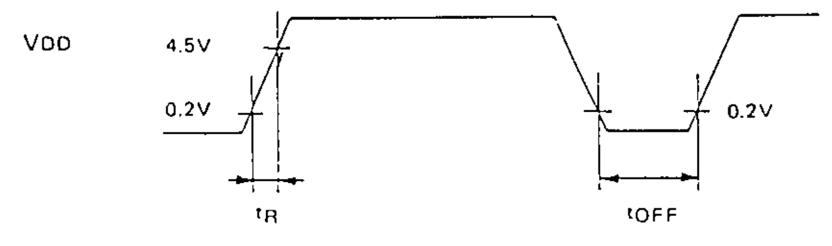
Fig. 9. Wake-up input timing

Power on reset *

(Ta=–20 to +75 ℃, Vss=0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
Power supply rising time	t_R	V_{DD}	Power on reset	0.05	50	ms
Power supply cut-off time	t_{OFF}		Repetitive power on reset	1		ms

* Specifies only when power on reset function is selected.



The power supply should rise smoothly.

Fig. 10. Power on reset

Notes on Application

See Fig. 11, Additive capacity calculation chart, when using the crystal oscillator and select the appropriate capacity.

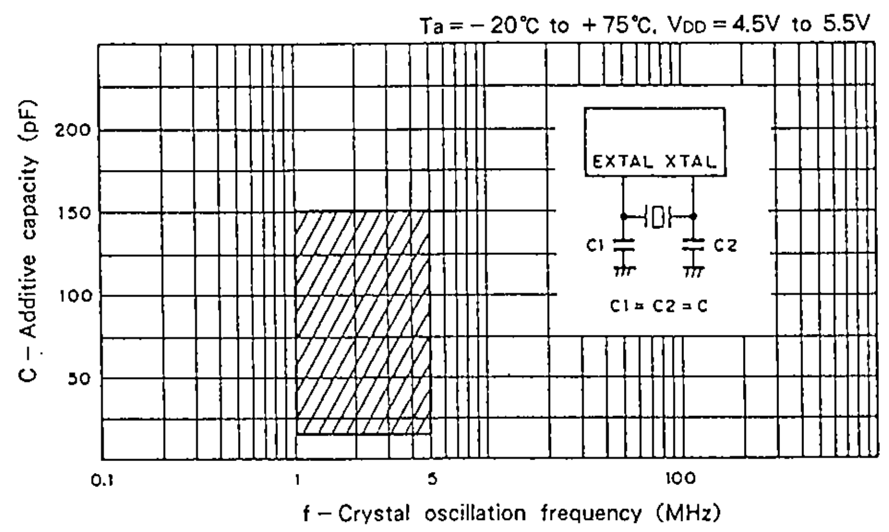


Fig. 11. Crystal oscillation circuit additive capacity calculation chart

Note) The above chart shows a range in which the average quartz resonator has a relatively fast oscillation rising edge and stable characteristics. The capacity should be selected to correspond to the appropriate constant for each quartz resonator, should the frequency of the quartz resonator be accurately adjusted.

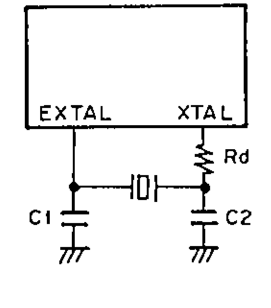
Fig. 12 shows recommended circuits and oscillators.
Use the trimmer capacitor to C1, in the case of accurate adjustment of the oscillation frequency.

1. Main clock

4.19MHz

Ceramic resonator

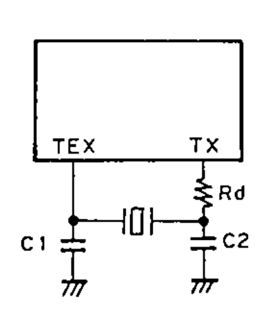
Manufacturer	Model	Frequency range(MHz)	C1 (pF)	C2 (pF)	Rd (Ω)
MURATA MFG CO., LTD.	CSA4.19MG040	4.19	100	100	——
	CSA4.19MGW040		built in	built in	——



Crystal oscillator

Manufacturer	Model	Frequency range (MHz)	C1 (pF)	C2 (pF)	Rd (Ω)
CITIZEN WATCH CO., LTD.	CSA309	4.19	10 (20 trimmer)	10	——
NIHON DEMPA KOGYO CO., LTD.	AT-51		15 (20 trimmer)	15	6.8k
KINSEKI LTD.	HC-49/U-S		22 (20 trimmer)	22	3.3k

2. 32kHz Timer/Counter



Manufacturer	Model	Frequency range (kHz)	C1 (pF)	C2 (pF)	Rd (Ω)
CITIZEN WATCH CO., LTD.	CFS-308	32.768	18 (20 trimmer)	18	——
NIHON DEMPA KOGYO CO., LTD.	MX-38T		22 (20 trimmer)	22	470k
KINSEKI LTD.	P3		22 (20 trimmer)	22	3.3k

About the details of oscillators, please inquire the makers or the agencies.

Fig. 12. Recommended oscillation circuit

When using the A/D converter as the key input, it is recommended that the circuit structure shown in Fig. 13 be used.

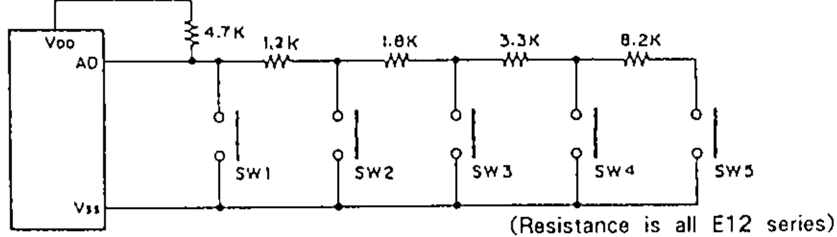
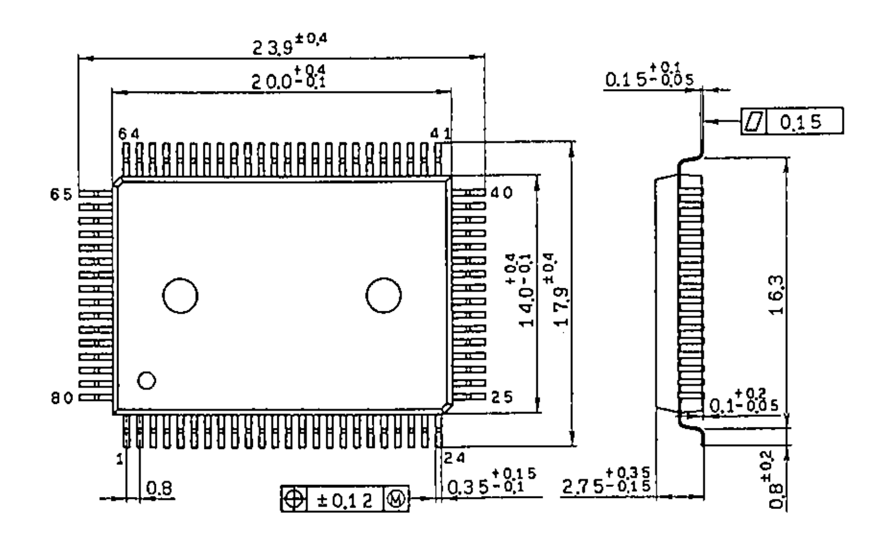


Fig. 13. Recommended example of key circuit by A/D converter

Package Outline Unit : mm

80pin QFP (Plastic) 1.6g



SONY NAME	QFP-80P-L01
EIAJ NAME	*QFP080-P-1420-A
JEDEC CODE	———